How far can we push Si CMOS?
What lies beyond?

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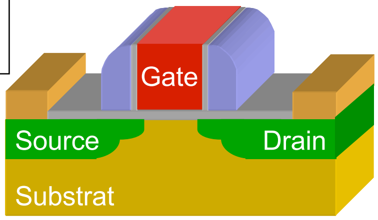
Physical Limits in Scaling Si MOSFET

Gate stack
- Tunneling current ⇒ ⇑ I_{off}
- Gate depletion ⇒ ⇑ EOT

Source/Drain
- Parasitic resistance
- Doping level, abruptness

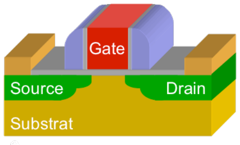


Power ⇑
- CV^2f ⇑
- S/D leakage current ⇑
- Gate leakage current ⇑

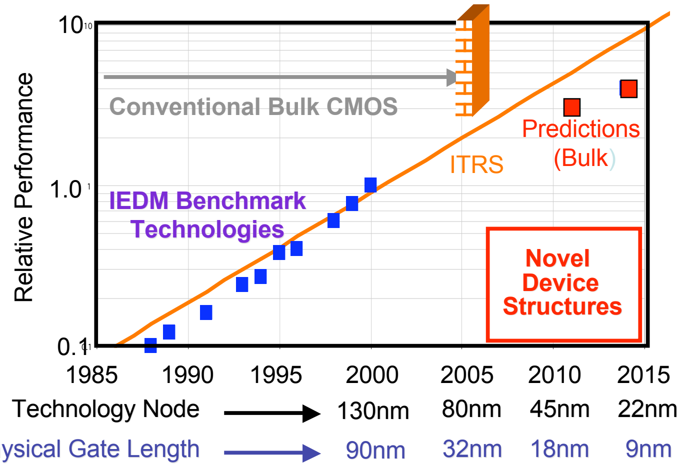
Channel/Drain
- Surface scattering - mobility ⇓
- High E-field - mobility ⇓
- DIBL ⇒ drain to source leakage ⇑ I_{off}
- Subthreshold slope $\geq kT/q$ ⇒ ⇑ I_{off}
- $V_G - V_T$ decrease ⇒ ⇓ I_{ON}

Net result: *Bulk-Si CMOS device performance increase commensurate with size scaling is unlikely beyond the 65 nm node*

Bulk-Si Performance Trends

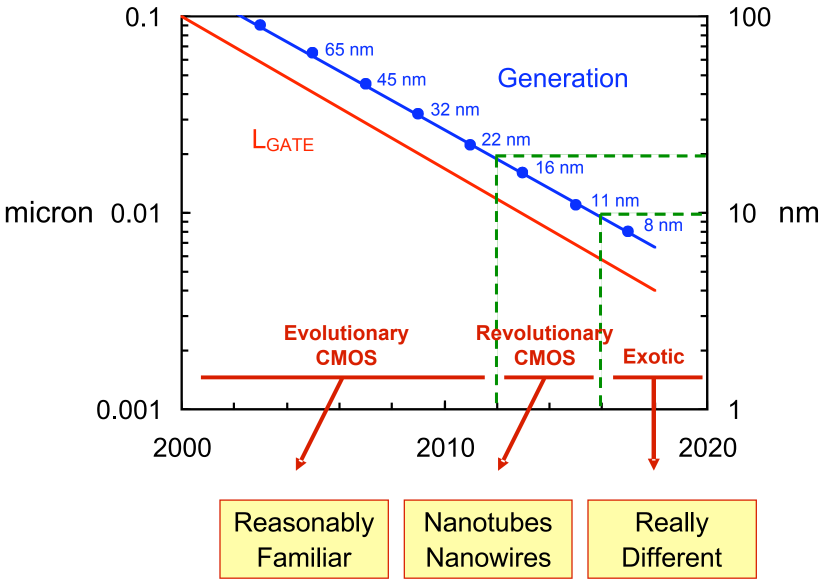


MOSFET in Bulk Si



- **Maintaining historical CMOS performance trend requires new semiconductor material and structures by 2008-2010…**
- **Earlier if current bulk-Si data do not improve significantly**

Nanotechnology Eras



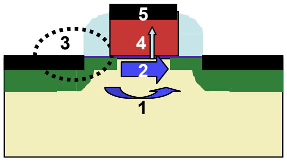
Source: Mark Bohr, Intel

Extending CMOS

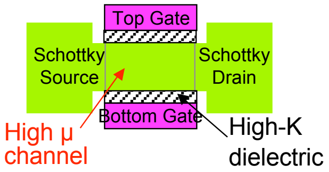
- Novel transistor structures and materials integration can extend *commensurate* CMOS scaling beyond planar bulk-Si solutions:
  - Improved Electrostatics and Contacts
    - Double-gate or surround-gate
    - Schottky source/drain
  - Improved Materials Properties
    - High mobility materials (e.g. strained Si/SiGe/Ge, etc.)
- Extended CMOS functionality via new Integration Technologies
    - 3-D Integration (Billions of transistors on a chip)
- Exploration of *new frontier* devices
    - *Alternatives compatible with silicon*

New Structures and Materials for Nanoscale MOSFETs

CURRENT BULK MOSFET



FUTURE MOSFET



Problem 1: Poor Electrostatics ⇒ increased I_{off}
Solution: Double Gate
- Retain gate control over channel
- Minimize OFF-state drain-source leakage

Problem 2: Poor Channel Transport ⇒ decreased I_{on}
Solution - High Mobility Channel
- High mobility/injection velocity
- High drive current and low intrinsic delay

Problem 3: S/D Parasitic resistance ⇒ decreased I_{on}
Solution - Metal Schottky S/D
- Reduced extrinsic resistance

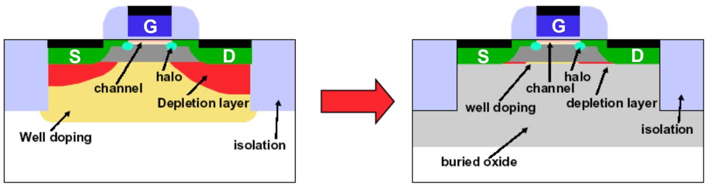
Problem 4. Gate leakage increased
Solution - High-K dielectrics
- Reduced gate leakage

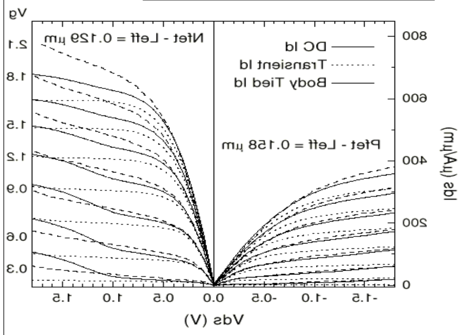
Problem 5. Gate depletion ⇒ increased EOT
Solution - Metal gate
- High drive current

Evolution of MOSFET Structures

Bulk

Partially Depleted SOI



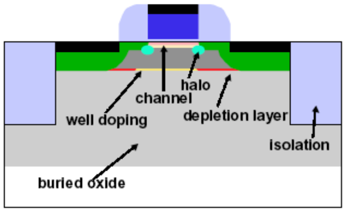


- Device design translates well between bulk and PD SOI
- e.g. short channel effect control by doping/halo (same as bulk)
- Reduced junction capacitances
- Dynamic floating body effect - parasitic bipolar

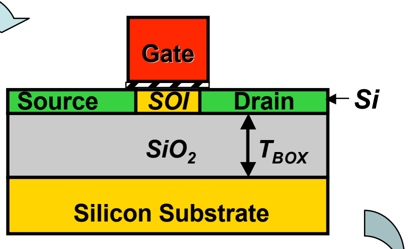
Ref: Philip Wong, IEDM Short Course, 1999

Evolution of MOSFET Structures

Partially Depleted SOI



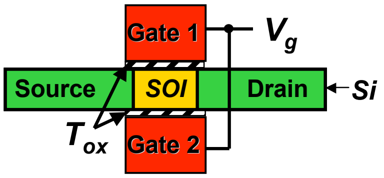
Ultra-Thin Body Single Gate SOI



Advantages of Ultra-Thin Body SOI

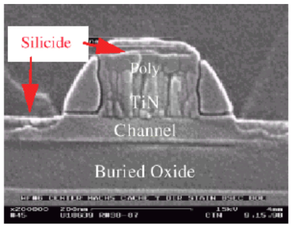
- **Depleted channel ⇒ no conduction path is far from the gate**
- **Short channel effects controlled by geometry**
- **Steeper subthreshold slope**
- **Lower or no channel doping**
  - **Higher mobility**
  - **Reduced dopant fluctuation**

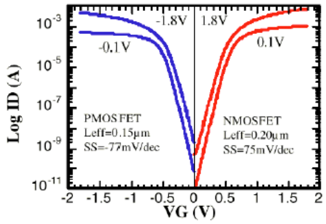
Ultra-Thin Body Double Gate SOI

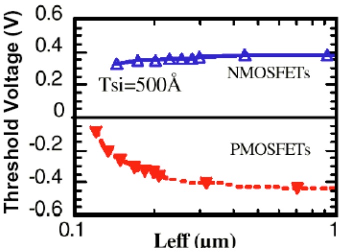


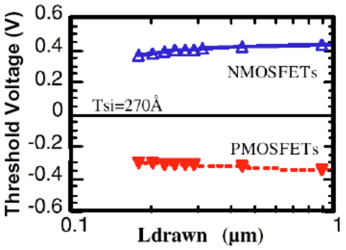
Ref: Philip Wong, IEDM Short Course, 1999

Fully Depleted SOI FET



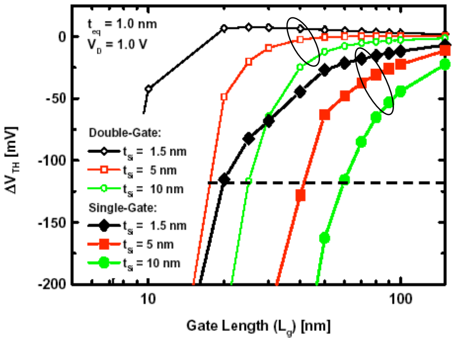




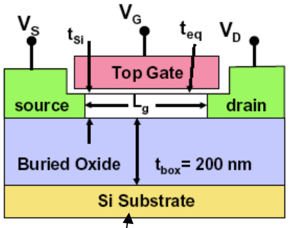


J. Chen et al., Symp. VLSI Tech., 1999.

Ultra-Thin Body Single vs. Double Gate SOI



H.-S. P. Wong, et al., p. 407, IEDM 1998.



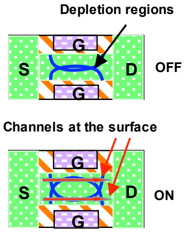
- Can be used as a second gate
- Not the ideal structure for double gate

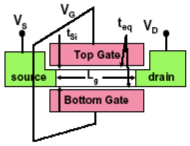
- In DG MOS better electrostatic control of the channel
  ⇒ Reduced short channel effects

Wong, et al. IEDM 1998

Double-Gate FET

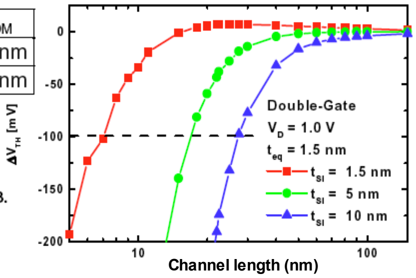
- ~2X current drive for the same device width
- Very thin (5 nm) undoped channel ⇒ better electrostatic control
  - ➢Steeper subthreshold slope - approaching 60 mV/dec
  - ➢Short-channel effect control feasible down to 20 nm
  - ➢May tolerate a thicker gate oxide for the same channel length
- Gate workfunction tuning needed for V_t control (for undoped channel)
- Steep lateral source/drain doping profile is required
- Parasitic source resistance
  - ➢Source/drain fan-out and contact - an integral part of the device structure



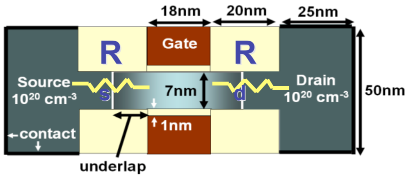


t_{Si}	L_{MIN}	L_{NOM}
5 nm	17 nm	22 nm
10 nm	27 nm	37 nm

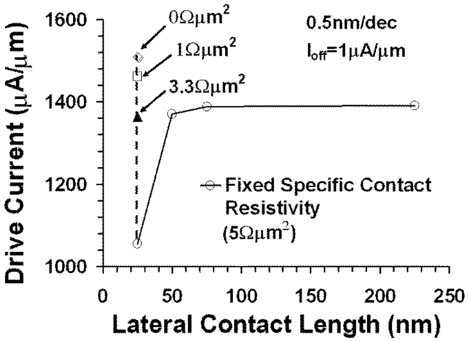
- H.-S. P. Wong, D. Frank, P. Solomon, p. 407, IEDM 1998.



Effect of Extrinsic Resistance on Double Gate FETs



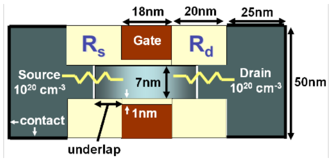
$$\boxed{I_d = K\cdot(V_g - V_{th} - I_d R_s)^{\alpha}}$$

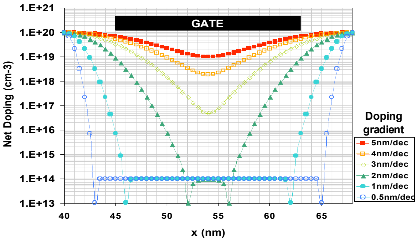


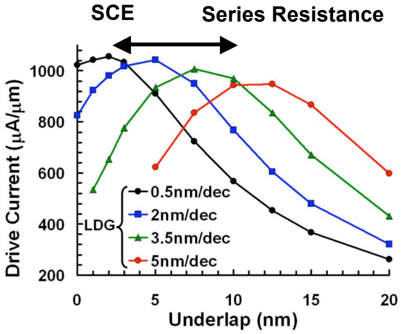
- Ultrathin body ⇒ higher series resistance
- More severe effect in Double-Gate FET
  - – Twice I_d flows through same Rs ⇒ higher series drop
- Degradation in I_{ON}
- **Need to reduce parasitic resistance**

Shenoy and Saraswat, IEEE Trans. Nanotechnology, Dec. 2003

Effect of Extrinsic Resistance on Double Gate MOSFETs





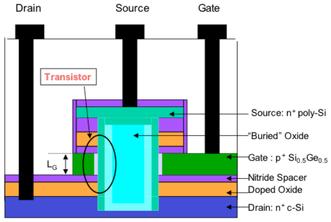


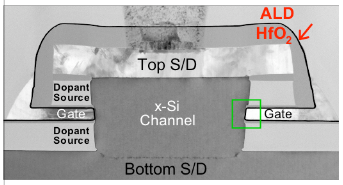
- **Extrinsic resistance reduces gate overdrive ⇒ performance limiter in ballistic FETs**
- **Doping profile too gradual: ⇒ dopants spill into channel ⇒ worse SCE**
- **Doping profile too abrupt: ⇒ large series resistance in extension tip**
- **Extrinsic (S/D) resistance may limit performance in future ultrathin body DGFETs**

Shenoy and Saraswat, IEEE Trans. Nanotechnology, Dec. 2003

Non Planar MOSFETs

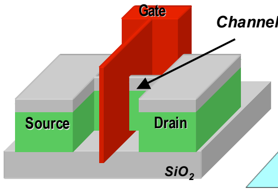
Vertical FET

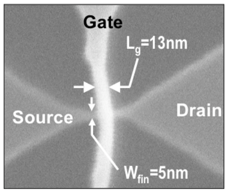




Stanford, AT&T

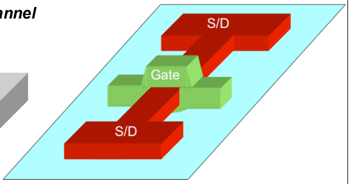
Double Gate FinFET

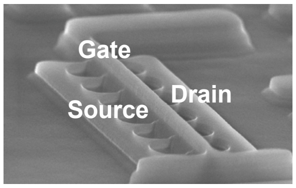




UC Berkeley

Tri Gate FET



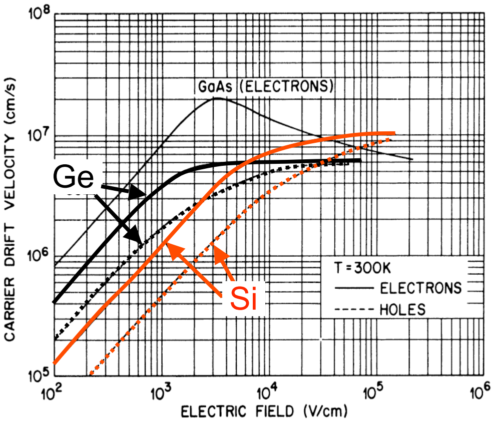


Intel

Why Germanium MOS Transistors?

Electronic Properties:

- More symmetric and higher carrier mobilities (low-field)
  - ⇒ More efficient source injection (due to lighter m^*)
  - ⇒ ↓ CMOS gate delay
- Smaller energy bandgap
  - ⇒ Survives V_{DD} scaling
  - ⇒ ↓ R with ↓ barrier height
- Lower temperature processing
  - ⇒ 3-D compatible



(Sze, *Phys. of Semicond. Devs. 2nd Ed.*, p.46, 1981)

CMOS Performance Boost with Ge

Drive Current & Gate Delay:

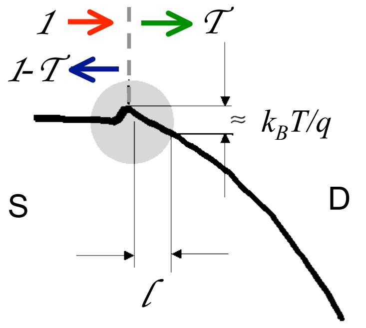
$$I_{ON} = \frac{W}{L_{gate}} \times Q_{inv} \times v_{inj}$$

$$\frac{C_{LOAD}V_{DD}}{I_D} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$

Ballistic Ratio Comparisons:
(from Monte Carlo simulations)

	Si <100>	Ge <100>	Ge <111>
n-MOS	0.68	0.78	0.76
p-MOS	0.48	0.70	0.56

MOSFET Channel Energy Band:



(Lundstrom *et al.*, 2001, Purdue)

$$\boxed{\mathcal{T} = \frac{\lambda_0}{l + \lambda_0}}$$

$$\boxed{\lambda_0 \propto \tau_0 \propto \mu_{low-field}}$$

Problems With Ge

Problems #1: Ge Surface Passivation

- The native oxide passivation on Ge surface is not stable enough either during fabrication or in the end-product

Solution:

- **High-κ** dielectrics are deposited on Si, why not on Ge?

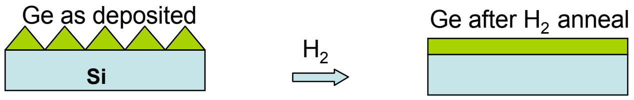
Problem #2: Ge Wafers as a Substrate?

- Ge substrate not easy to handle and not easily available
- Si will continue to be the main substrate due to its overall excellent properties

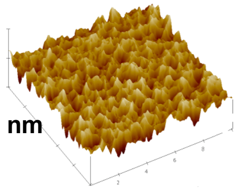
Solution:

- Heterogeneous integration of Ge on Si.

Heteroepitaxial Growth of Ge on Si

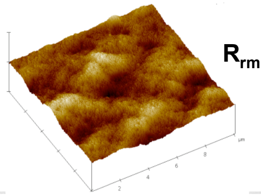


AFM



R_{rms} : 25 nm

Z = 50nm/div,
X= 2μm/div

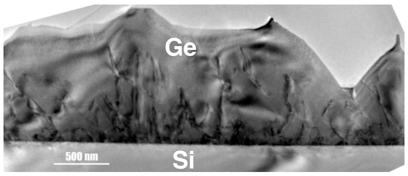


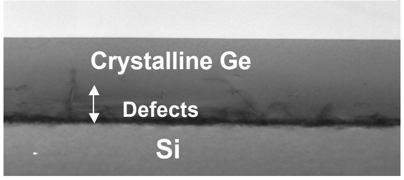
R_{rms} :2.5nm

As Grown at 400°C No H_2 Anneal

400°C Growth + 825˚C H_2 Anneal

TEM

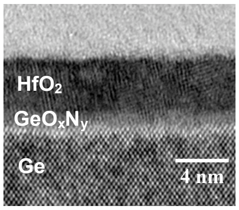




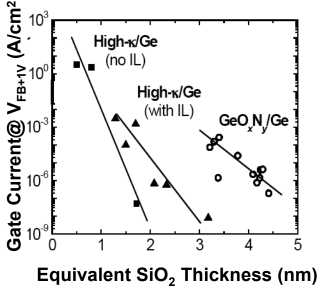
With H_2 anneal dislocations are confined to the Si/Ge interface leaving defect free top Ge layers.

High Mobility Ge FETs with High-k

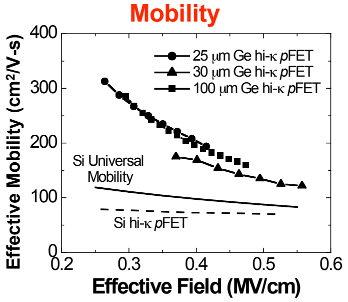
HR-XTEM



Gate Leakage



Mobility



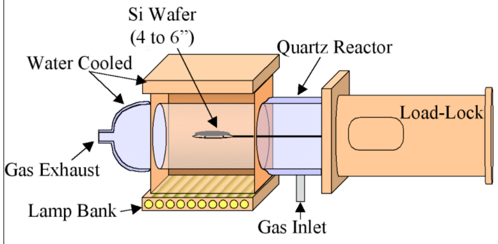
Key Results

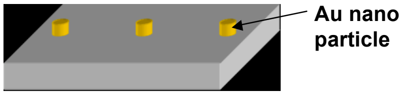
- Passivation of Ge with GeO_xN_y, ZrO_2 and HfO_2
- n and p dopant incorporation
- 1st demo of Ge MOSFETs with metal gate and hi-κ
- *p*-MOSFET with 3× mobility vs. Hi-k Si
- *n*-MOSFET demonstrated but mobility low

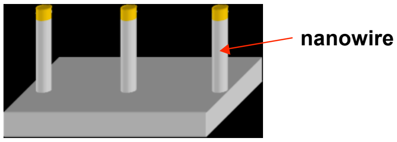
Chui, Kim, McIntyre and Saraswat, IEDM 2003

Ge nanowires synthesized by low temperature CVD

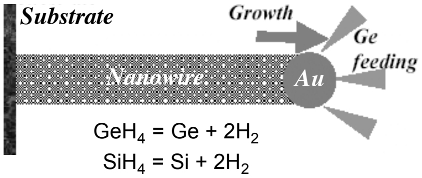
Cold-Wall NW Growth Reactor





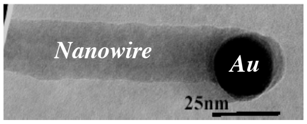


- Vapor-Liquid Solid (VLS) mechanism uses super saturated liquid eutectic to locally deposit Si.
- Growth mechanism: wires grow as the catalytic end moves
- Size of the wire is decides by the size of the nano particle
- 10-20 nm single crystal Ge wires
- CVD temperature: 275 - 400°C

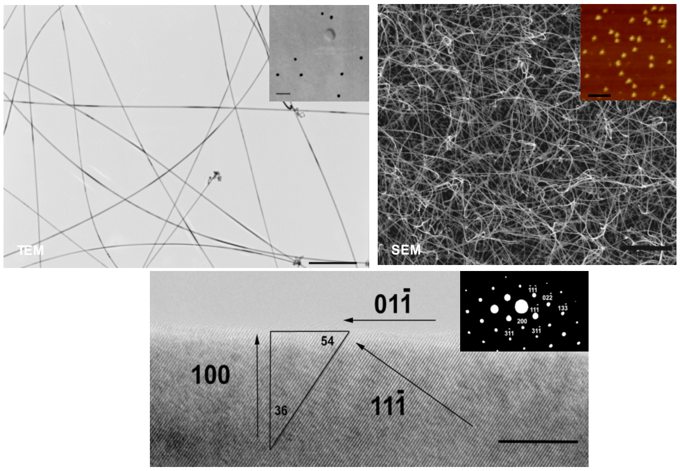


$GeH_4 = Ge + 2H_2$

$SiH_4 = Si + 2H_2$



Ge Nanowire Growth

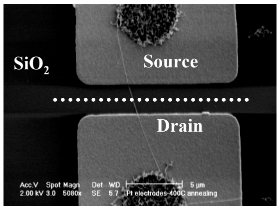


- No control over the overall growth direction
- Individual wires are single crystal and grow along <110> direction

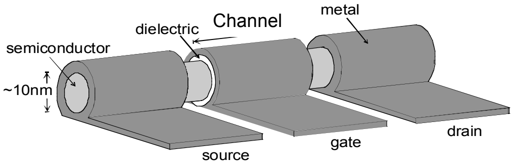
Courtesy: Hongjie Dai

Ge Nanowire FET with High K gate dielectric

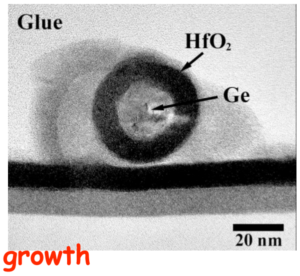
Top view SEM



Ge NW MOSFET



ALD HfO_2 Coating of Ge NW



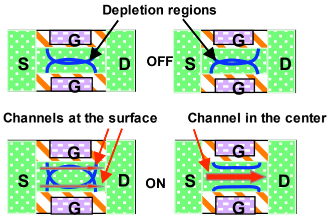
- 10-20 nm single crystal Ge wires
- CVD temperature: 275 °C
- Initial fabricated transistor shows great promise μ_p ~ 500
- 3D integrable technology

Key Challenge: Controlled growth

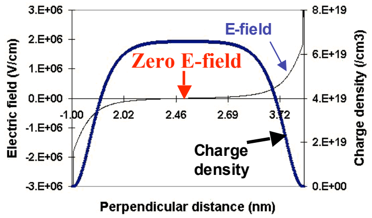
Ref: Wang, Wang, Javey, Tu, Dai, Kim, McIntyre, Krishnamohan, and Saraswat, Appl Phys. Lett, 22 Sept. 2003

Center Channel Double/Surround Gate FET

Conventional DG **Depletion-Mode DG**



Schred: 1-D Poisson-Schrodinger simulations



Transport:

- Zero E-field by symmetry of DG structure
- Reduced scattering due to perpendicular E-field
- Natural fan-out (lower $R_{parasitic}$)

Technology integration:

- Easier integration with high-k materials
- Fully utilizes excellent transport properties of materials like Ge, SiGe, strained Si etc.

Electrostatics:

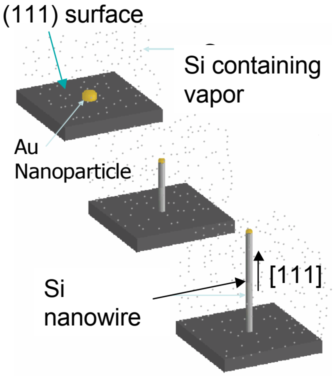
- Excellent control of short channel effects due to DG structure
- Excellent sub-threshold slope
- Very low DIBL and V_{th} roll-off

High performance devices:

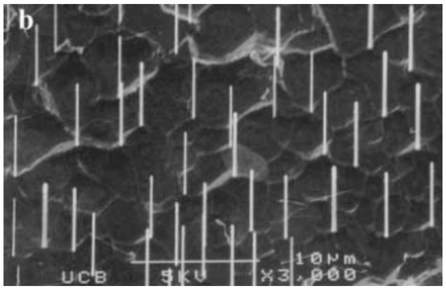
- High mobility channels leading to very high drive currents
- Very high switching speeds
- Very high cut-off frequencies
- Lower power dissipation

Krishnamohan and Saraswat, IEDM 2003

Epitaxial Growth of Vertical Nanowires

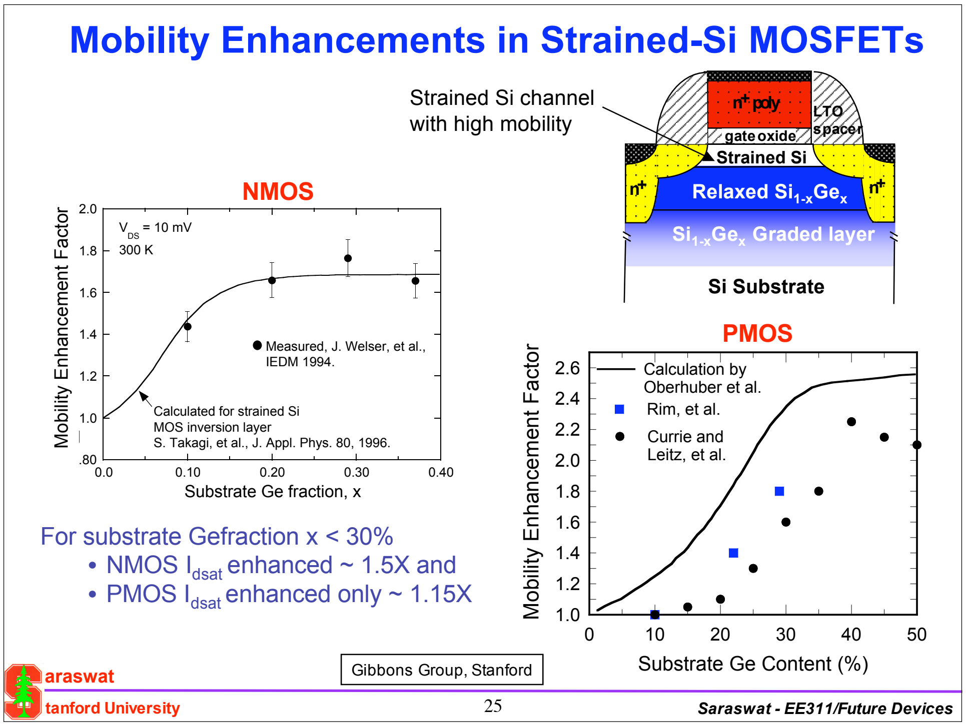


<111> oriented Si NWs on (111) Si



Yiying Wu et al., Chem. Eur. J., 2002, 8, 1261

Si nanowires grow epitaxially on a (111) Si plane

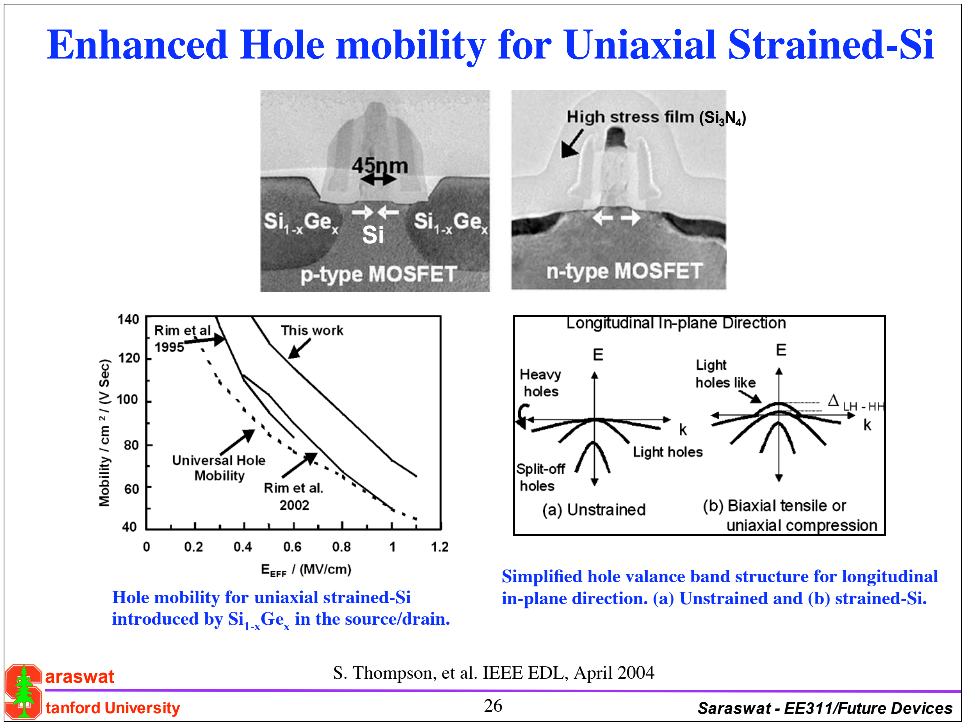


Mobility Enhancements in Strained-Si MOSFETs

For substrate Gefraction x < 30%

- NMOS I_{dsat} enhanced ~ 1.5X and
- PMOS I_{dsat} enhanced only ~ 1.15X

Gibbons Group, Stanford

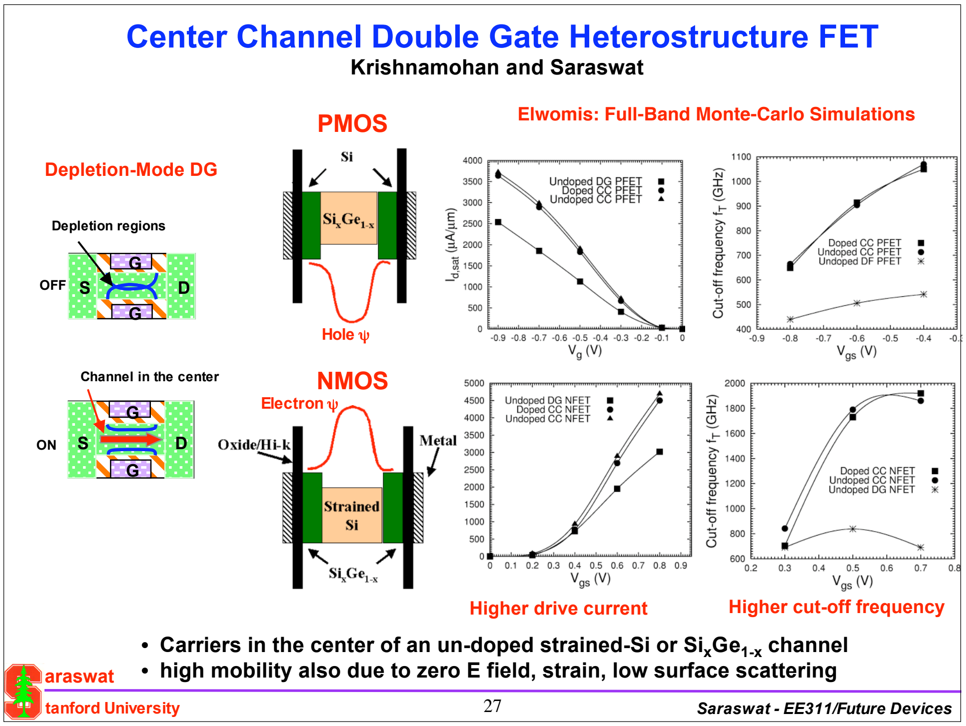


Enhanced Hole mobility for Uniaxial Strained-Si

Hole mobility for uniaxial strained-Si introduced by $Si_{1-x}Ge_x$ in the source/drain.

Simplified hole valance band structure for longitudinal in-plane direction. (a) Unstrained and (b) strained-Si.

S. Thompson, et al. IEEE EDL, April 2004



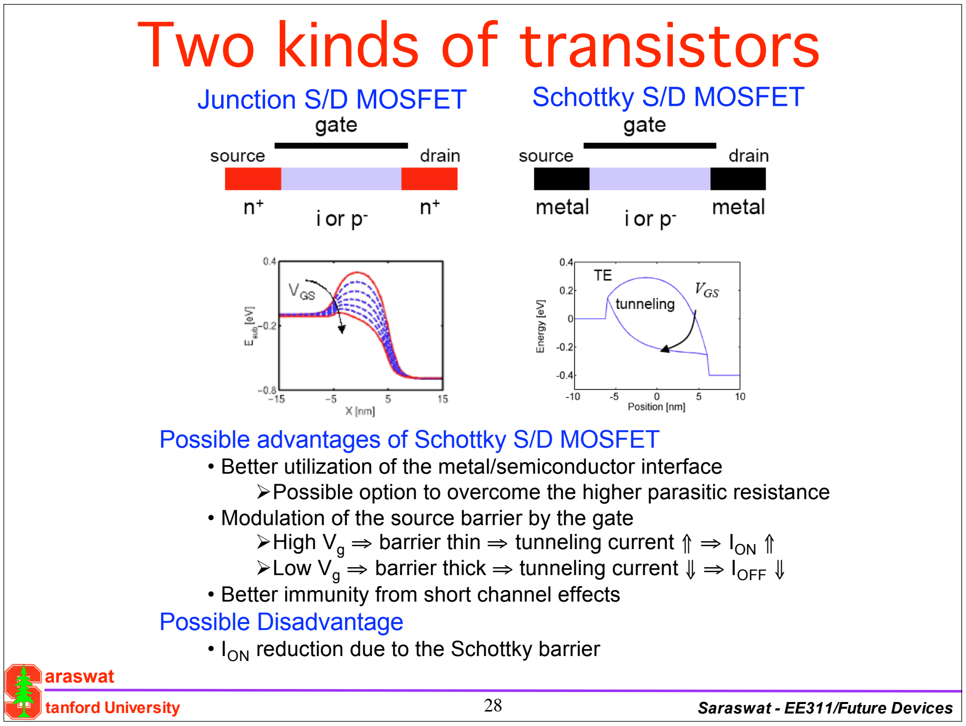
Center Channel Double Gate Heterostructure FET

Krishnamohan and Saraswat

Higher drive current

Higher cut-off frequency

- **Carriers in the center of an un-doped strained-Si or Si_xGe_{1-x} channel**
- **high mobility also due to zero E field, strain, low surface scattering**



Two kinds of transistors

Possible advantages of Schottky S/D MOSFET

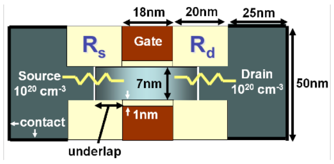
- Better utilization of the metal/semiconductor interface
  - ➢Possible option to overcome the higher parasitic resistance
- Modulation of the source barrier by the gate
  - ➢High V_g ⇒ barrier thin ⇒ tunneling current ⇑ ⇒ I_{ON} ⇑
  - ➢Low V_g ⇒ barrier thick ⇒ tunneling current ⇓ ⇒ I_{OFF} ⇓
- Better immunity from short channel effects

Possible Disadvantage

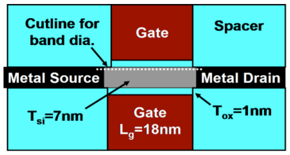
- I_{ON} reduction due to the Schottky barrier

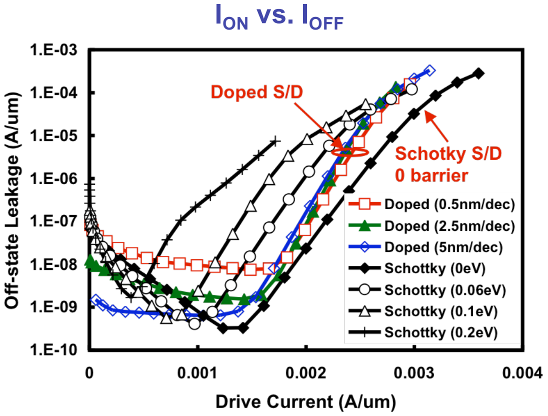
PN Junction vs. Schottky S/D Si DGFET Simulations

PN Junction S/D



Schottky S/D

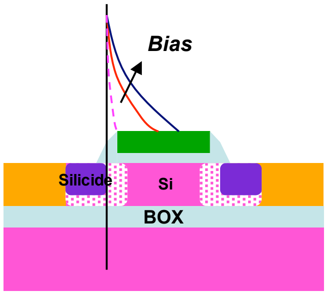


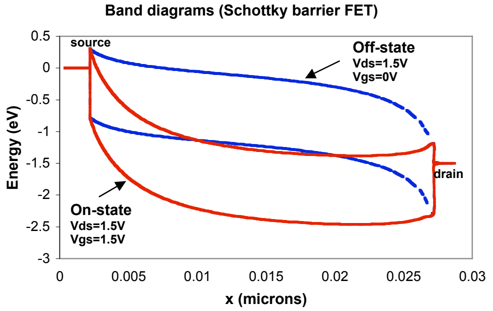


Low barrier height metal/semiconductor contacts required to achieve high I_{ON} and low I_{OFF}

R. Shenoy, PhD Thesis, 2004

Schottky Barrier MOSFET



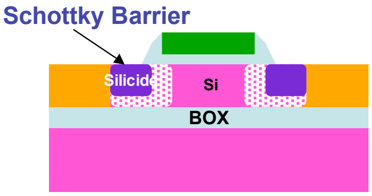


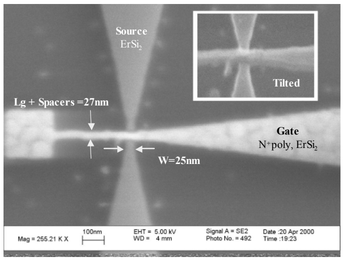
Possible advantages
- Better utilization of the metal/semiconductor interface
  - ➢Possible option to overcome the higher parasitic resistance
- Modulation of the source barrier by the gate
  - ➢High $V_g \Rightarrow$ barrier thin $\Rightarrow$ tunneling current $\Uparrow \Rightarrow I_{ON} \Uparrow$
  - ➢Low $V_g \Rightarrow$ barrier thick $\Rightarrow$ tunneling current $\Downarrow \Rightarrow I_{OFF} \Downarrow$
- Better immunity from short channel effects

•Disadvantage
- Tradeoff between short channel effect vs. I_{ON} reduction due to the Schottky barrier

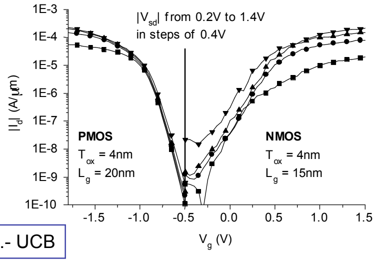
Optimal ϕ_B Schottky Barrier MOSFET

L_g~20 nm FETs with Complementary Silicides PtSi PMOS, ErSi NMOS





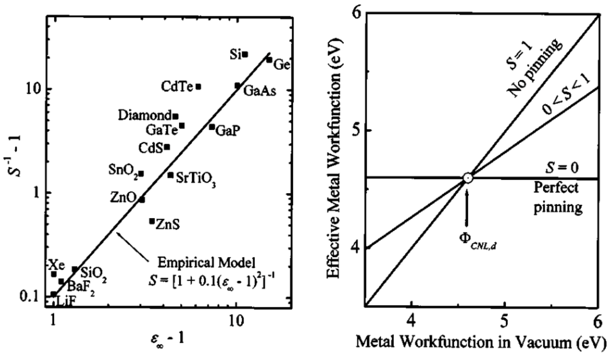
	PtSi PMOS	ErSi NMOS
Lg	20 nm	15 nm
Tox	4 nm	4 nm
Vg-Vt	1.2 V	1.2 V
Ion	270 uA/um	190 uA/um
Swing	100 mV/dec	150 mV/dec
Ion/Ioff	5E5	1E4
Vt	-0.7 V	-0.1 V

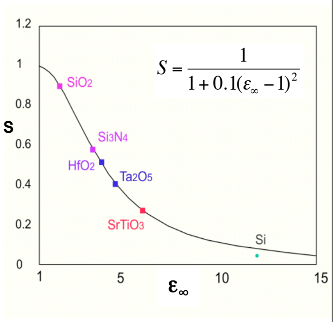


- Metal S/D reduce extrinsic resistance
- Need ultrathin channel, double gate
- Need low barrier technology to ensure high I_{on}

J. Boker et al.- UCB

Variation of the Schottky barrier *S* factor





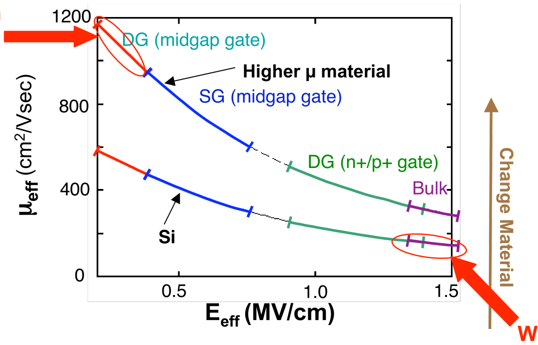
Yeo, King, and Hu, J. Appl. Phys., 15 Dec. 2002

Ref: Robertson, MRS March 2005

- High K's are less 'Schottky-like' than SiO_2. Barrier heights change less than metal workfunction.
- Strong pinning for semiconductors

Combining New Device Structures with New Materials

We will be here with these innovations

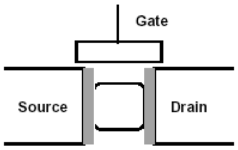


We are here today

Change Architecture allows reduced doping

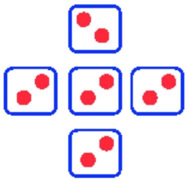
- With better injection and transport we may be able to reach closer to the ballistic I_{on}
- With better electrostatics we may be able to minimize I_{off}

Seemingly Useful Devices



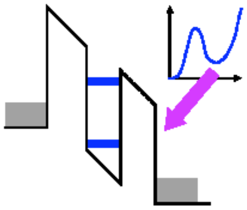
Single Electron Transistors (SET)

Limited Current Drive
Cryogenic operation



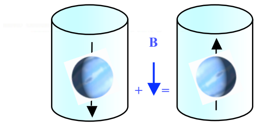
Quantum Dot

Limited Fan-Out
Critical dimension control



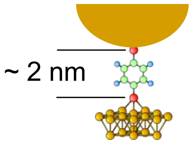
Resonant Tunneling Diode

Challenging fabrication and process integration



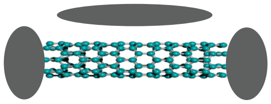
Spintronics

Need high spin injection and long spin coherence time



Molecular Device

Limited thermal stability
New architectures needed

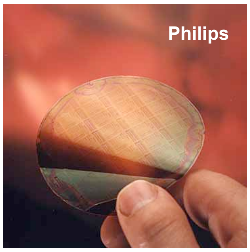


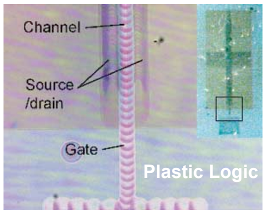
Carbon Nanotubes

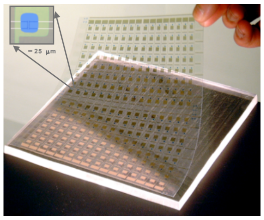
Controlled growth

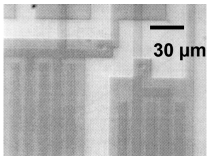
Motivation for Organic FETs

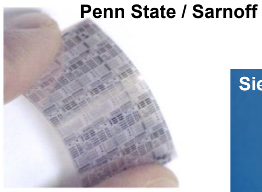
Low-Cost, Flexible Electronics



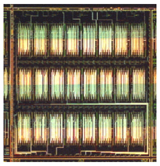








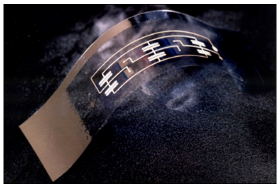
Organic Semiconductors



LSI
(864 Transistors)

B. Crone, A. Dodabalapur et al.
Nature **403**, 521 (2000)

All-Printed Polymer Circuit
Z. Bao / Bell Labs



Applications

- **identification tags**
- **low-end data storage**
- **smart cards**
- **emissive displays**
- **electronic paper**
- **distributed computing**
- **toys, clothes, ...**

low-cost, lightweight, rugged, flexible electronics

No competition to Si,
Going where Si can't follow !!

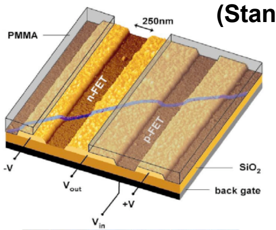
Next Step : ‘Molecular Electronics

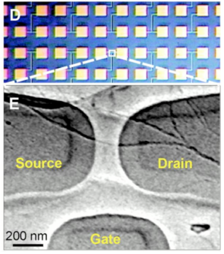
Nanotube Devices / Circuits

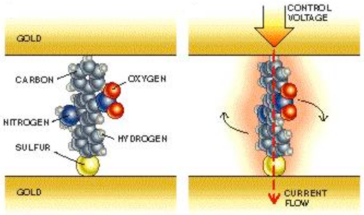
(Stanford, IBM, ...)

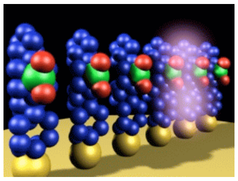
Molecular Switches

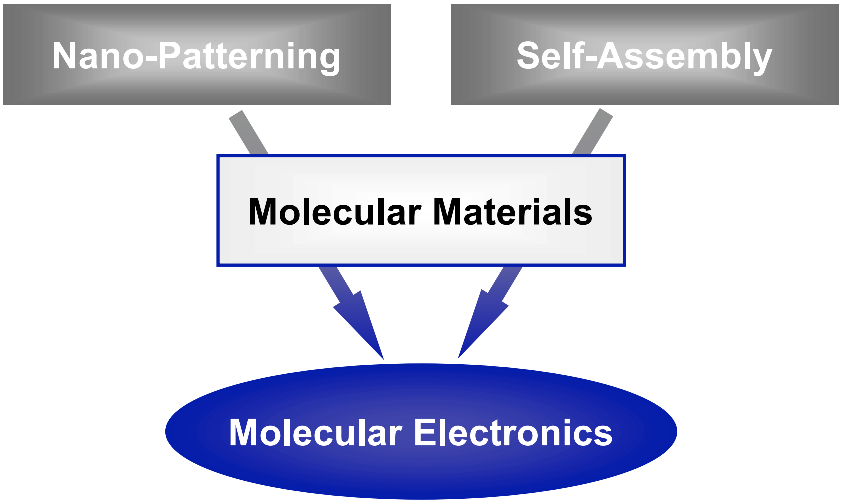
(HP, Cal Tech, Stanford ...)











Nano-Patterning

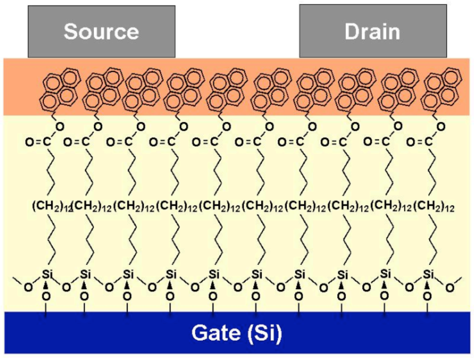
Self-Assembly

Molecular Materials

Molecular Electronics

Molecular-Scale Three-Terminal Devices ?

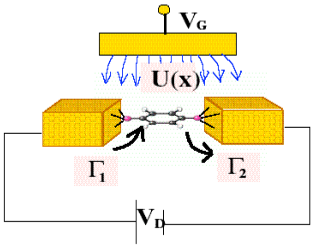
Organic Insulator / Semiconductor Monolayer
($\sigma - \pi$ SAM)



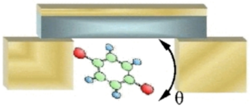
J. Collet et al., APL **76**, 1339 (2000).

Self-Assembled Monolayer Molecular FET

Molecular FETs

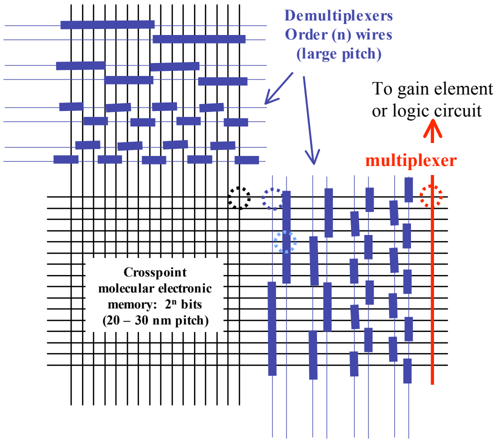


Molecular Relays

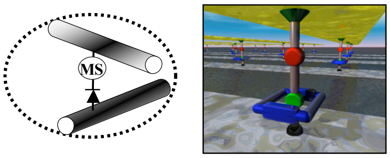


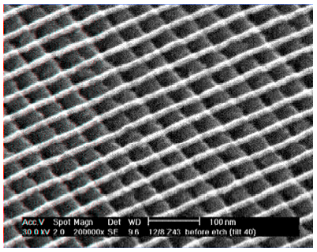
- **Molecular Length Defines Channel**

Molecular Electronics Interfaced with Silicon Technology



Molecular Switch

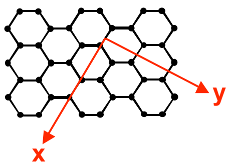


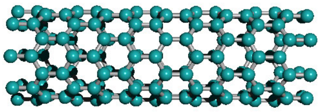


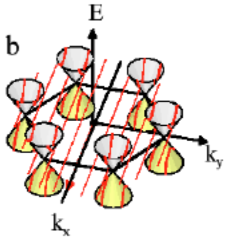
- **Molecular mechanical complexes as solid-state switch elements**
- **Non-traditional patterning techniques to achieve a memory bit (cross-point) density of >10^{11}/cm^2.**
- **Non-linear, voltage response of molecular switches to latch (amplify) and clock signals by coupling a large molecular circuit with very few CMOS-type amplifiers.**

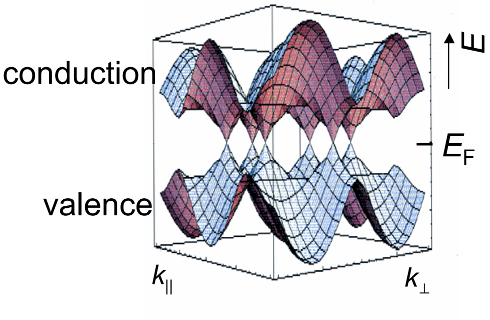
Source: Nicholas Melosh and J. Heath

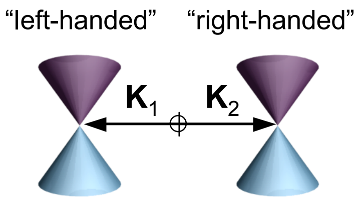
Graphene band structure





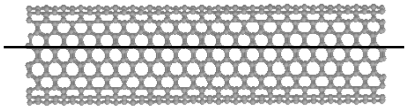




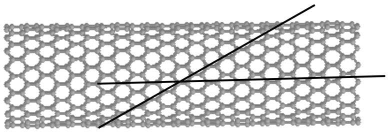


Two cones in unit cell
Symmetry $\mathbf{K}_1 = -\mathbf{K}_2$

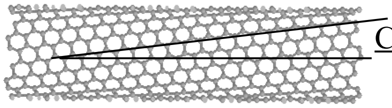
Diversity of SWNTs



(10,10) Arm-chair
Metal



(18,0) Zig-zag
Small gap
Quasi-metal

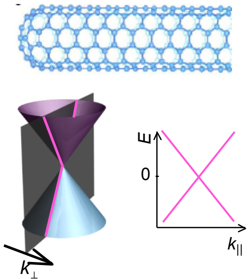


(7,12)
Chiral
Semiconductor

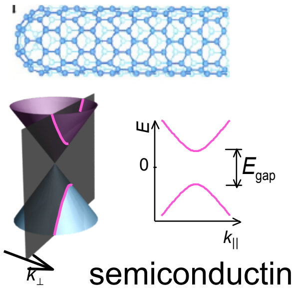
Chiral angle: M, S, or Quasi-M

Diameter: band gap ~ $1/d$
(0.6 eV for d=1.4 nm)
(0.84 eV for d=1 nm)

Nanotube Band Structure



metal

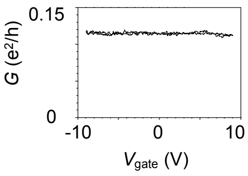


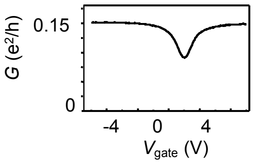
$E_g \approx 0.8/d$ (nm) eV)

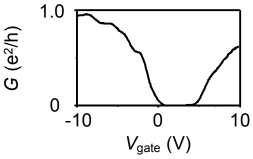
semiconducting

small bandgap semiconducting

large bandgap semiconducting

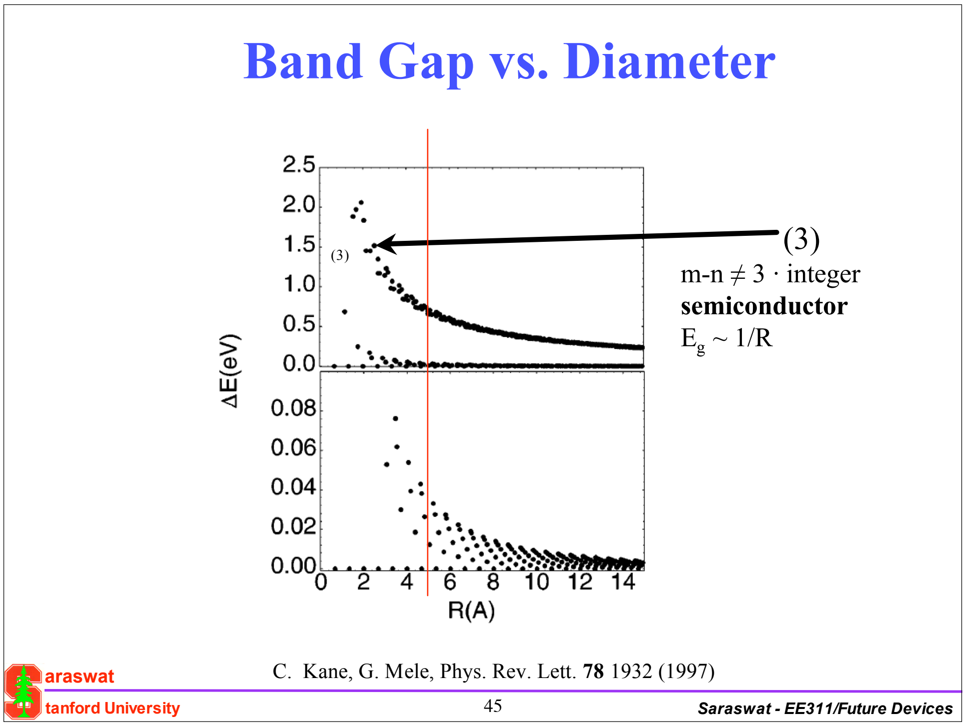






Due to curvature, strain, etc.

McEuen et al., *IEEE Trans. Nanotech.*, 1 , 78, 2002.



Band Gap vs. Diameter

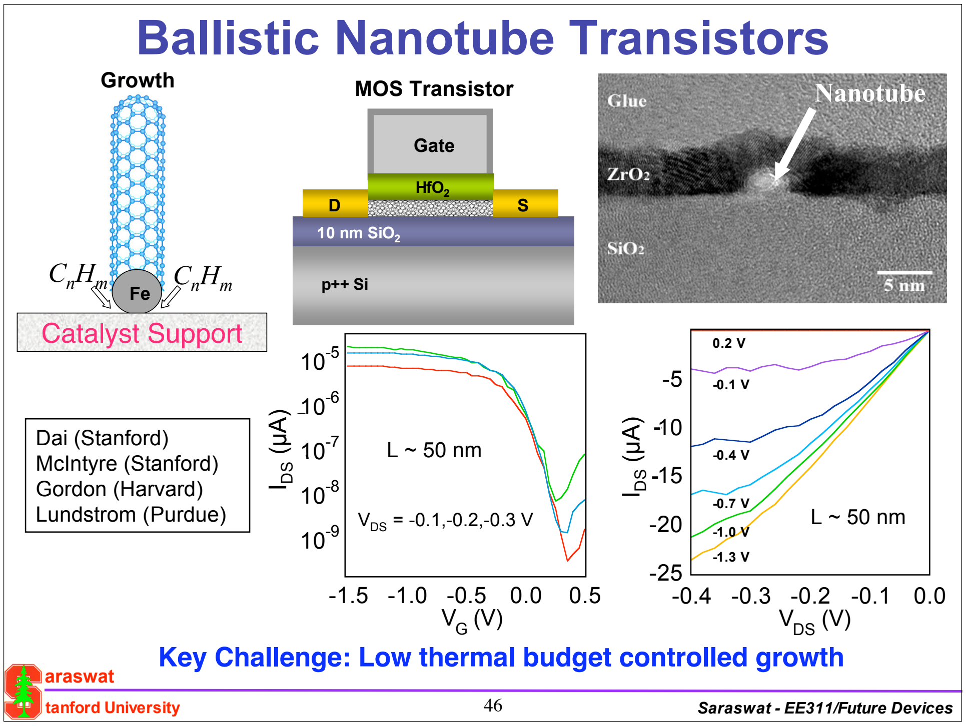
(3)

m-n ≠ 3 · integer

semiconductor

$E_g \sim 1/R$

C. Kane, G. Mele, Phys. Rev. Lett. **78** 1932 (1997)

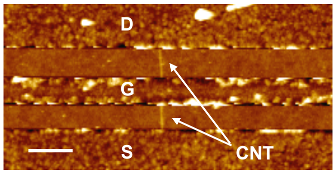


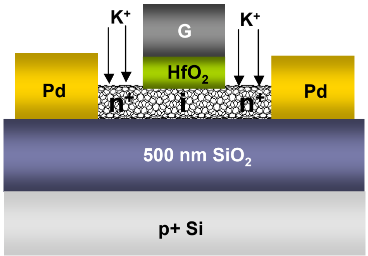
Ballistic Nanotube Transistors

Dai (Stanford)
McIntyre (Stanford)
Gordon (Harvard)
Lundstrom (Purdue)

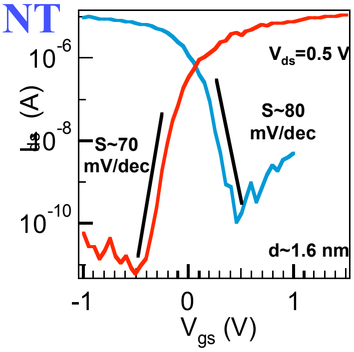
Key Challenge: Low thermal budget controlled growth

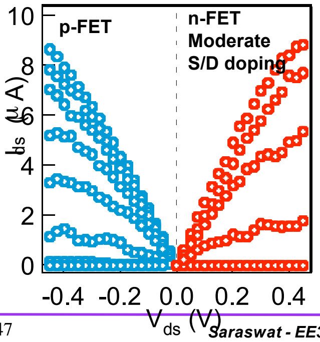
High Performance CNT N-MOSFETs



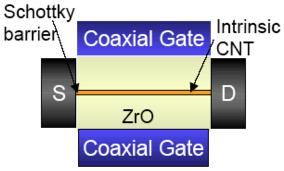


Dai/Gordon/Guo Groups



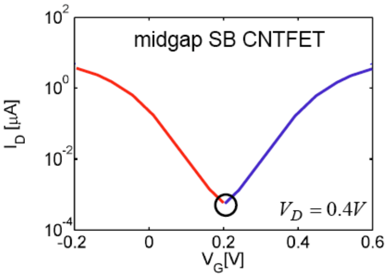


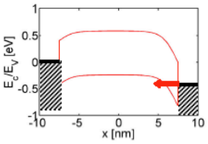
Ambipolar Schottky S/D Nanotube FETs



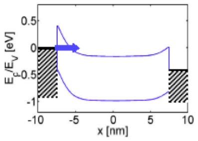
Schottky barrier CNTFET

Heinze et al, "Carbon nanotubes as Schottky barrier transistors", *PRL*, **89**, 106801,2002



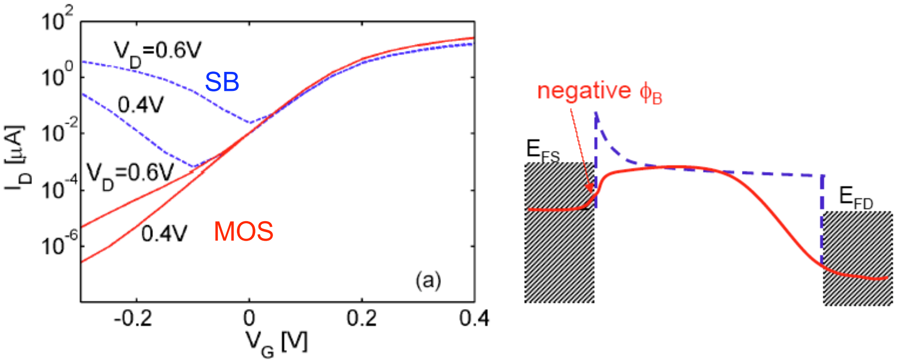


$V_G < V_D/2$
hole conduction



$V_G > V_D/2$
electron conduction

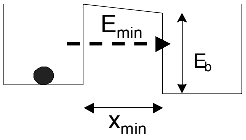
Conventional MOS Like Nanotube FETs



Dai group, Stanford

Theoretical Limits to Scaling

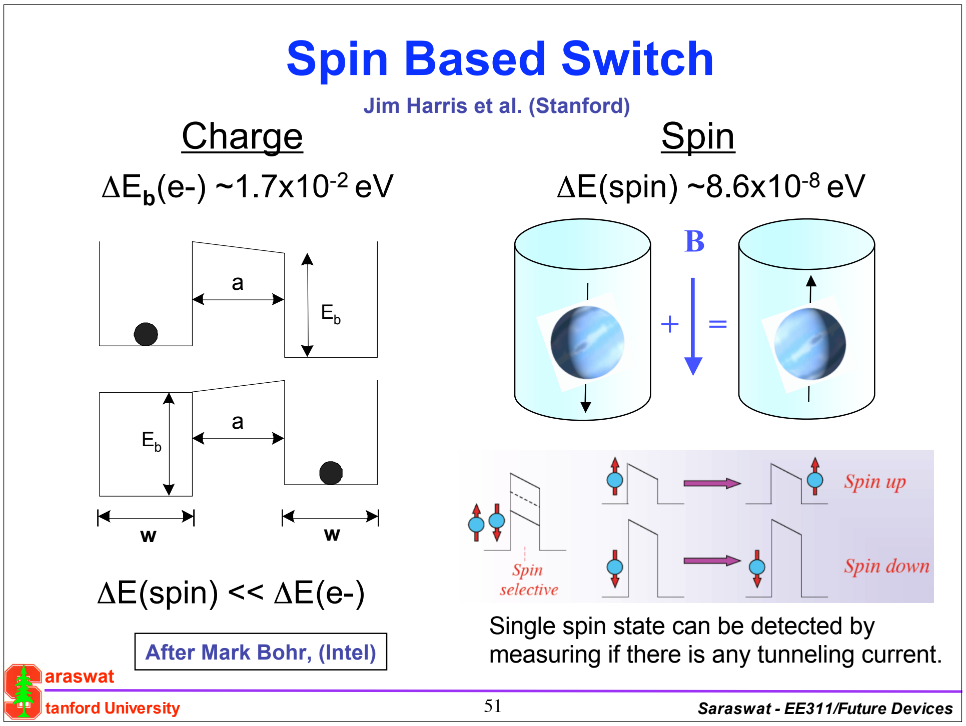
- Thermodynamic limit:
  $E_b \geq k_B.T.\ln 2$
- Quantum mechanics
  $\Delta x \,.\, \Delta p \geq h$ ➠ x_{min} (Integration density)
  $\Delta E \,.\, \Delta t \geq h$ ➠ τ (witching speed)



- Ultimate limit:
  - x_{min} ~ 1.5 nm ➠ 5.10^3 transistors/cm^3
  - Switching speed t_{min} ~ 0.04 ps ➠ 25 Tbits/sec
  - Switching energy E_{bit} = 17 meV
  - Power = 55 nW/bit
- For densely packed, 100% duty cycle devices
  - Total power density = 4.10^6 W/cm^2
- With duty cycle ~1 %, Active transistors ~1 %
  - Total power density = 370 W/cm^2

$$P = \frac{n_{\max} E_{bit}}{t_{\min}}$$

Source: George Bourianoff, Intel



Spin Based Switch

Jim Harris et al. (Stanford)

<u>Charge</u>

$\Delta E_b(e^-) \sim 1.7 \times 10^{-2}$ eV

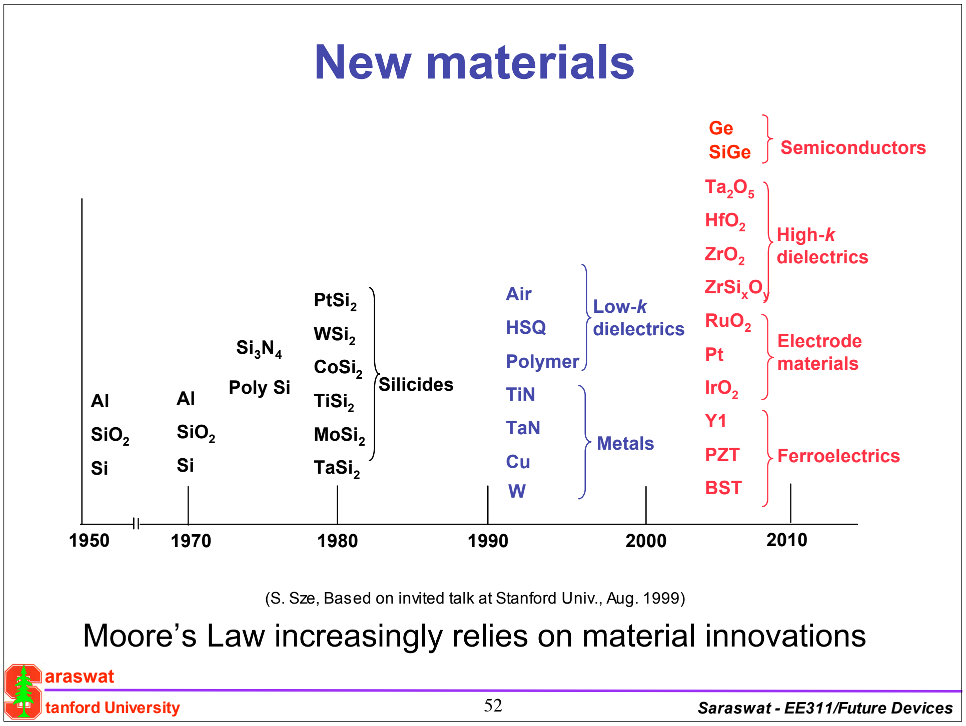
$\Delta E(\text{spin}) \ll \Delta E(e^-)$

After Mark Bohr, (Intel)

<u>Spin</u>

$\Delta E(\text{spin}) \sim 8.6 \times 10^{-8}$ eV

Single spin state can be detected by measuring if there is any tunneling current.



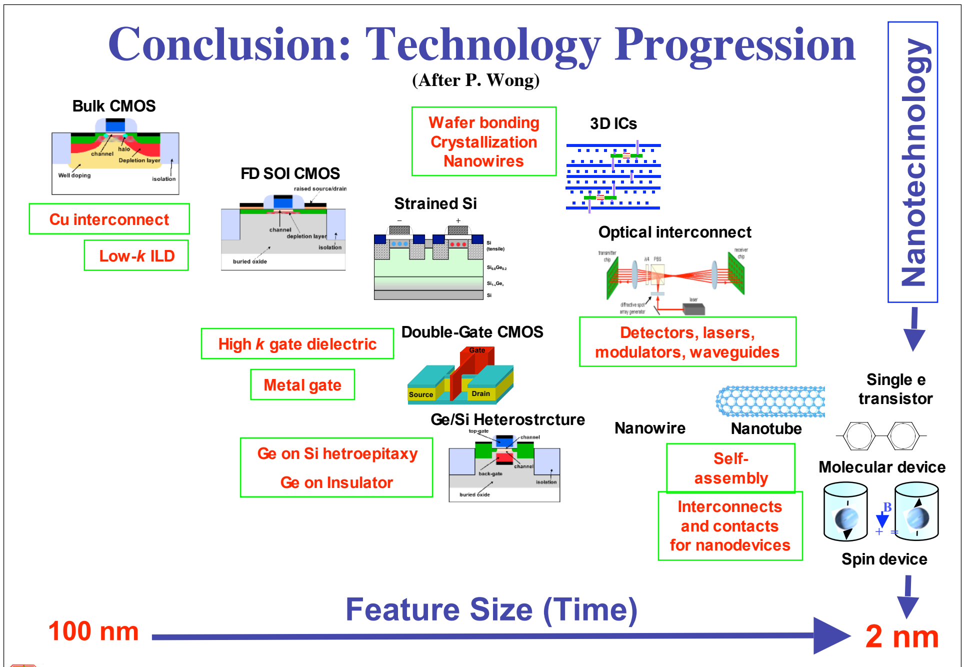
New materials

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Moore's Law increasingly relies on material innovations

Conclusion: Technology Progression

(After P. Wong)



Cu interconnect

Low-*k* ILD

Wafer bonding
Crystallization
Nanowires

High *k* gate dielectric

Metal gate

Detectors, lasers, modulators, waveguides

Ge on Si hetroepitaxy

Ge on Insulator

Self-assembly

Interconnects and contacts for nanodevices